Amendments to the Claims

1. *(Currently Amended)* A circuit comprising a first ~~(10)~~ and a second circuit module ~~(20)~~ and a synchronization module ~~(30),~~ the first and the second module being mutually a-synchronous, and being coupled by the synchronization module, the synchronization module ~~(30)~~
comprising
a transfer register ~~(3 1)~~ for storing data which is communicated between the two circuit modules,
a control circuit ~~(32)~~ for controlling the register in response to a respective timing signal (Stl, St2) from the first and the second circuit module, the control circuit comprising a control chain for generating a control signal (CR) for the transfer register ~~(3 1),~~ the control chain including at least
- a repeater ~~(34)~~ for inducing changes in the value of the control signal,
- at least one edge sensitive element ~~(35)~~ for delaying a change in the signal value until a transition in a selected one of the timing signals is detected.

2. *(Currently Amended)* A circuit according to claim 1, further comprising a comparator ~~(136)~~ for generating a difference signal (AD) upon detection of a difference between an input and an output of the transfer register ~~(131),~~ the control chain further comprising a wait element ~~(137)~~ for delaying an active transition in the control signal until a difference is detected.

3. *(Currently Amended)* A circuit according to ~~claim 1 or 2~~claim 1 wherein the control chain further comprises an arbitration element ~~(138),~~ the arbitration element having respective channels for guiding at least a first and a second signal flow, the arbitration element being arranged for arbitrating between passing active events in the first and the second signal flow, the first channel being arranged between an output of the edge sensitive element~~(135)~~ and an input of the repeater ~~(134).~~

4. *(Currently Amended)* **A** circuit according to claim 3, wherein the selected timing signal is a clock signal (Wclk) from the first circuit module ~~(110),~~ wherein the timing signal from the second circuit module ~~(120)~~ is an access request signal (Rreq), the second channel of the arbitration element ~~(138)~~ having a first input for receiving the access request signal (Rreq) and a first output for providing an access acknowledge signal (Rack) to the second circuit module ~~(120).~~

5. *(Currently Amended)* A circuit according to claim 3, further comprising an auxiliary register ~~(431B)~~ for transferring data from the first module ~~(410)~~ to the register ~~(431),~~ wherein the selected timing signal is a clock signal (Rclk) from the second circuit module ~~(420),~~ wherein the timing signal from the first circuit ~~(410)~~ module is a write request signal (Wreq), the second channel of the arbitration element ~~(438)~~ having a second input **(c)** for receiving the write request signal and a second output **(d)** for providing a control signal to control the auxiliary register ~~(431B).~~

6. *(Currently Amended)* A circuit according to ~~claim 1 or 2~~claim 1 wherein the selected one of the timing signals is a clock signal (Wclk) from the first circuit module ~~(210),~~ the circuit including an auxiliary register ~~(231A)~~ for transferring data from the transfer register ~~(231)~~ to

the second circuit module ~~(220),~~ and wherein the circuit includes a further edge sensitive element ~~(235A)~~ for delaying a change in a control signal for the auxiliary register ~~(231A)~~ until a transition is detected in a timing signal (Rclk) from the second circuit module ~~(220).~~

7. *(Currently Amended)* A circuit according to claim 6, wherein the further edge sensitive element ~~(337A)~~ is part of the control chain.

8. *(Currently Amended)* A circuit according to claim 6, wherein the further edge sensitive element ~~(237A)~~ is part of a further control chain, which is coupled to the control chain.

9. *(Currently Amended)* A circuit according to ~~claim 1 or 2~~claim 1, wherein the synchronization module has a first transfer register ~~(3 1)~~ for transferring data from the first ~~(10)~~ to the second circuit module ~~(20)~~ and a second transfer register ~~(33)~~ for transferring data from the second ~~(20)~~ to the first circuit module ~~(10),~~ the transfer registers ~~(31,22)~~ being controlled by the same control signal ~~(CR).~~

10. A method for transferring data between a first ~~(10)~~ and a second circuit module ~~(20)~~ using a synchronization module ~~(30),~~ the first and the second module being mutually a-synclwonous, and being coupled by the synchronization module, the method comprising the following steps

- temporarily storing data which is transferred from the first to the second circuit module in a register,

-controlling the register in response to a respective timing signal from the first, and the second circuit module, by a control circuit which comprises a control chain for generating a control signal wherein

- changes are induced in the value of the control signal,
- a change in the signal value is delayed until a transition in a selected one of the timing signals is detected.